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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SIXTH SEMESTER B.TECH DEGREE EXAMINATION, APRIL 2018

Course Code: EC304

Course Name: VLSI (EC)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks. Marks

1 a) Illustrate with diagram the principle of crystal growth by Czochralzki method. (5)

b) What is photolithography? With diagram illustrate the steps involved in photolithography process. (5)

c) A SiO_2 layer is grown by wet oxidation at 1000°C for 40 minutes followed by dry oxidation for 1 hour at 1200°C. Determine the thickness of the oxide layer formed. For wet oxidation at 1000°C, B=0.29 , B/A=1.27 and for dry oxidation at 1200°C , B= 0.045, B/A= 1.120 , $\tau = 0.027$ (5)

2 a) What is Deal Grove model of oxidation? What are linear and parabolic rate coefficients with reference to oxidation process? (5)

b) Explain the principle of molecular beam epitaxy, with schematic diagram of an MBE system. What are its advantages and disadvantages? (5)

c) A silicon crystal is to be grown by Czochralski process and is to contain 5×10^{15} boron atoms/cm^3. Given the segregation constant k_0 for Boron in silicon is 0.8. Atomic weight of boron equals 10.81g/mole, density of silicon 2.22g/cm^3 and Avogadro number is 6.023×10^{23} atoms/mole. (a) Determine the initial concentration of Boron in the melt to produce the required doping density. (b) If the initial amount of silicon in the crucible is 20kg, how many grams of Boron should be added to obtain the same doping? (5)

3 a) With schematic diagram and chemical reactions involved, illustrate wet and dry oxidation processes. (5)

b) Determine the ratio of Silicon consumed to the thickness of grown SiO_2 layer over silicon wafer. If SiO_2 layer of 0.2 µm is to be grown, what would be the thickness of used up Silicon. Molecular weight of SiO_2 = 60.08g.mole, density of SiO_2=2.2g/cm3, atomic weight of Si=20.09 and density of Si= 2.33g/cm^3 (5)

c) What are the different methods of fabricating capacitors in integrated circuits? Illustrate with diagrams. (5)

PART B

Answer any two full questions, each carries 15 marks.

4 a) What are the different types of power dissipation in a CMOS inverter? Derive expression for the total power dissipation. (10)

b) Realise a THE FUNCTION f= AB'C+A C(DE+A'B) using standard CMOS logic. (5)

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5 a) Draw the circuit diagram and layout of a 4 input NAND gate. (10)

b) What is meant by pass transistor logic? What are the differences in transmission characteristics of N MOS and P MOS transistors? (5)

6 a) Derive expression for the switching threshold of a CMOS inverter. (5)

b) What is layout design rule? What are the differences between λ rule and micron rule? (5)

c) Draw the circuit diagram of an Ex-OR gate in pass transistor logic. (5)

PART C

Answer any two full questions, each carries 20 marks.

7 a) Draw the circuit diagram and explain the principle of operation of a CMOS based static RAM cell. Explain the read and write operations. What are the constraints on the sizes of transistors? (10)

b) With block diagram illustrate the principle of operation of a square root carry select adder. Estimate the delay of an n bit adder (10)

8 a) Draw circuit diagram of a full adder with not more than 28 transistors in standard CMOS logic. (10)

b) What is FPGA? What are its applications? With block diagram explain its internal architecture? (10)

9 a) Draw the circuit diagram and explain the principle of operation of a one transistor dynamic RAM cell. Explain the read, write and refresh operations. (10)

b) With diagram illustrate the principle of operation of an array multiplier. Show the critical path. Estimate the delay of the multiplier. (10)

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